ABSTRACT

A data processor for efficiently processing a large amount of data at high speed by using a processor, like an arithmetic process of motion vector estimation in an image process. An SDMD ALU 4 controlled by a CPU 2 and a work RAM 12 are connected via a local bus 8 having a bus width wider than a bus width of a data bus 6 of the CPU 2, an address bus 18 is commonly connected to the SDMD ALU 4, the work RAM 12, and the CPU 2, and the SDMD ALU 4 and the work RAM 12 are controlled by the CPU 2 in a centralized manner, thereby realizing a high speed data process.